# Highly Robust All-Oxide Transistors with Ultrathin $In_2O_3$ as Channel and Thick $In_2O_3$ as Metal Gate Towards Vertical Logic and Memory

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## Abstract

In this work, we report atomic-layer-deposited (ALD) all-oxide transistors toward 3-D vertical integration, with thick ALD $In_2O_3$ as gate electrodes, and $In_2O_3$ itself as contact. The all-oxide thin-film transistors (TFTs) show an on/off ratio over $10^6$, high uniformity, and very robust reliability with a threshold voltage shift ($\Delta V_{TH}$) of 5 mV and 50 mV in positive and negative bias stress (PBS and NBS) tests. The vertically full-oxide TFTs demonstrate good control from side wall with on/off ratio over $10^5$ and maximum current ($I_{max}$) over 160 μA/μm. And vertically all-oxide ferroelectric field-effect transistors (Fe-FETs) exhibit a memory window (MW) of 1.85 V, with an endurance and retention extended to $10^{12}$ cycles and 10 years. This illustrates the vertically all-oxide device based on ALD oxide semiconductor (OS) is a good candidate toward future high-density integrated circuits.

## Introduction

Neural network (NN) has achieved a significant breakthrough in accelerating intelligent tasks. To keep enhancing energy efficiency of computing, new strategies such as in-memory computing are proposed, which is gradually making high-density memory density a necessity. One promising solution for this demand is to stack memory cells in 3-D form vertically. In terms of vertical memory cells of both mainstream and emerging technology, such as DRAM and Fe-FETs, although devices have been demonstrated in conventional semiconductors, such as poly-Si and Si/SiGe [1-6], they usually suffer from less-ideal sidewall uniformity, variation on doping profile, and high thermal budgets and metal diffusion under high-temperature treatment. In contrast, ALD based OS, such as $In_2O_3$ and $InGaZnO_x$ (IGZO), have been recently noticed as a suitable channel material for monolithic 3-D integration, due to their 3-D conformality, high current, high-quality contact, and back-end-of-line compatibility [7-10]. While most reports on vertical OS TFTs include metallization process [11-13], by replacing conventional metal or nitride metal gate with thick degenerated $In_2O_3$ gate, both yield and reliability can be enhanced for the absence of metal diffusion with a great simplification of process. Meanwhile, the fabricated all-oxide transistors can satisfy the transparency requirement for 3-D NN in display or transparent flexible electronics applications shown in Fig. 1.

In this work, we report ALD-based all-oxide transistors toward 3-D vertical integration, using degenerated ALD $In_2O_3$ as conducting gate, and ALD $In_2O_3$ itself as contact without metal contact formation. Such fabricated all-oxide TFTs with post-deposition annealing (PDA) in $O_2$ at 400 °C or more show high uniformity and very robust reliability with a $\Delta V_{TH}$ of 5 mV and 50 mV in PBS and NBS tests. Vertically all-oxide TFTs demonstrate good control from side wall with on/off ratio > $10^5$ and $I_{max}$ >160 μA/μm. ALD vertical Fe-FETs exhibit a MW of 1.85 V, with a high endurance extended to $10^{12}$ cycles and long retention extended to 10 years at room temperature.

## Experiments

Figs. 2 and 3 show the device schematic diagram and fabrication process flow of all-oxide planar or vertical TFTs and Fe-FETs all based on ALD $In_2O_3$.10 nm $In_2O_3$ grown by ALD at 225 °C is used as the oxide conducting gate ($T_{IO,g}$=10 nm). The two steps in star, deep trenching followed by top $Al_2O_3$ spacer deposition, are special for vertical structure. The electrical characterization was carried out with the Keysight B1500 Semiconductor analyzer in a Cascade probe station, using tip directly probing on $In_2O_3$ film.

## Results and Discussion

To assess the process impact on an all-oxide device, planar TFTs were investigated as reference. Fig. 4 shows the transfer characteristics of an all-oxide planar TFT with channel length ($L_{ch}$) of 2 μm, channel thickness ($T_{ch}$) of 2.6 nm and without PDA treatment. Devices show an on/off ratio of $10^6$ at $V_{DS}$ of 1 V. 30 devices randomly from four 0.5-by 0.5-μm dies are measured with a low variability. Fig. 5 shows the evolution of transfer curves with PDA treatment at various temperatures. Devices have a higher on/off ratio after PDA. Figs. 6 (a)-(d) present the statistical plots of threshold voltage ($V_{TH}$), subthreshold swing (SS), on-state current ($I_{ON}$) and on-state transconductance ($g_{m,ON}$) of as-deposited all-oxide TFT and devices with PDA at temperature from 400 to 490 °C. The $V_{TH}$ of TFTs approaches enhancement-mode with SS approaching 60 mV/dec after high-temperature PDA, while without significant on-state degradation. Variability of TFTs is also improved after 400 °C PDA. This implies the superiority of all-oxide process over metallization process for building OS-TFTs on interface quality and device performance under high-temperature treatment, due to the absence of interface degradation from metal diffusion. Fig. 7 shows the output characteristics of an all-oxide planar TFTs with $L_{ch}$ of 2 μm, $T_{ch}$ of 2.6 nm and with PDA at 490 °C. Device show a good saturation behavior with $I_{D,max}$ over 65 μA/μm. To further investigate the contact of a full-oxide TFT, Schottky barrier height ($\Phi_{SB}$) was extracted from the temperature-dependent transfer curves of an all-oxide planar TFT with PDA at 400 °C in Fig. 9 and Fig 8, respectively. The inset of Fig. 8 shows the Arrhenius plot at different gate biases extracted from Fig. 10 [13]. The $\Phi_{SB}$ was extracted to be slightly negative at flat-band condition, illustrating an excellent contact quality even without S/D metallization.

Figs. 10(a) and (b) presents the evolution of $I_D$-$V_{GS}$ curves of a full-oxide planar TFT with and without PDA at 490 °C under PBS ($V_{GS}$ of 3 V) and NBS ($V_{GS}$ of -3 V) test for 10000 s, respectively. Fig. 11 shows the extracted $\Delta V_{TH}$ over stress time. The full-oxide TFTs show highly robust reliability after $O_2$ PDA at 490 °C with $\Delta V_{TH}$ of 5/50 mV under PBS/NBS condition. These results imply the full-oxide TFT based on ALD OS a good candidate toward highly robust vertical structure.

Fig. 12 shows the high-resolution transmission electron microscopy (HRTEM) cross section view with EDS mapping of an ALD vertically all-oxide TFT with $T_{IO,g}$ of 10 nm to control the thin $In_2O_3$ channel on the side. The top $Al_2O_3$ layer exists only in HRTEM sample for protection. Figs. 13 and 14 present the typical transfer and output characteristics of an ALD vertical all-oxide TFT with $T_{IO,ch}$ of 1.6 nm, $L_{ch}$ of 16 μm, and $T_{IO,g}$ of 10 nm. The device exhibits an on/off ratio over $10^5$, suggesting an effective gate control of the $In_2O_3$ channel on the vertical side wall. Fig. 15 shows the output characteristics of a vertical TFT with $L_{ch}$ of 1 μm. The device reaches an $I_{max}$ of 160 μA/μm. It needs to be noted that the maximum drain current is pinned by two planar link parts, as shown in Fig. 2, due to a weak gate modulation, which can be improved by further scaling down the channel length. Device simulation confirms the experimental observation and points out the stronger modulation on the link resistance on source side vs. drain side shown in Fig. 2. Fig. 16 shows the $\Delta V_{TH}$ under PBS condition on vertical all-oxide TFTs with $In_2O_3$ and IGZO channel. Without PDA, compared with $In_2O_3$, IGZO channel presents a higher reliability under the same biasing conditions with a cost of on-state performance degradation.

The all-oxide vertical structure also enables high-performance Fe-FETs. Fig. 17 demonstrates a typical transfer characteristic with counter-clockwise hysteresis loop with $L_{ch}$ of 1 μm, showing a MW of 1.85 V. Fig. 18 shows the endurance and retention of the same vertical all-oxide Fe-FET. The endurance was measured to be $10^9$ cycles without significant degradation and can be extended to $10^{12}$ cycles at room temperature. The retention time was measured and can be extended to 1000 s and10 years, respectively. The classical metal-oxide-semiconductor interfaces become oxide-oxide-oxide interfaces.

## Conclusion

In conclusion, ALD-based all-oxide transistors toward 3-D vertical integration are demonstrated, using thick degenerated ALD $In_2O_3$ as gate electrodes, and $In_2O_3$ itself as contact, without metallization. The vertical all-oxide TFTs demonstrate good control from side wall with on/off ratio over $10^5$ and $I_{max}$ over 160 μA/μm. And vertical all-oxide Fe-FETs exhibit a MW of 1.85 V, with an endurance extended to $10^{12}$ cycles and long retention extended to 10 years. This work demonstrates that the vertical all-oxide devices are good candidates toward future 3-D high-density ICs. The work is supported by Samsung Electronics.

**Reference:** [1] Y. Kurita et al., TED, 32, 3, p. 657, 2009. [2] H. Chung *et al.*, *ESSDERC*, pp. 211, 2011. [3] J. S. Shin et al., EDL, 33, 2, p. 134, 2012. [4] K. Florent et al., IEDM, 2.5, 2018. [5] K. Banerjee et al., IMW, pp. 1–4, 2021. [6] W. Huang et al., EDL, 43, 11, p. 1874, 2022. [7] M. Si et al., VLSIT, TF2-4, 2021. [8] Z. Lin et al., ACS Nano, 16, p. 21536, 2022. [9] Z. Zhang et al., VLSIT, TF11-3, 2023. [10] C. Niu et al., IEDM, 37.2, 2023. [11] M.-K. Kim *et al.*, *Sci. Adv.*, eabe1341, 2021. [12] X. Duan et al., TED, 69, 4, p. 2196, 2022. [13] Z. Li *et al.*, EDL, 43, 8, p. 1227, 2022.

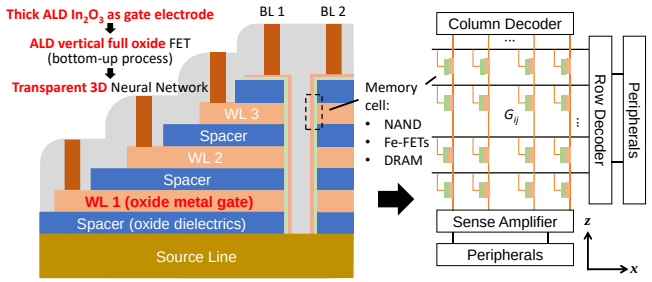


Fig. 1. Motivation of this work: a 3D vertical array of ALD all-oxide transistors using thick conducting ALD $In_2O_3$ as gate electrode. This design simplifies the fabrication process and enhance reliability against metal diffusion.

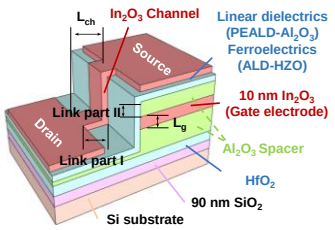


Fig. 2. 3-D device schematic of an ALD vertical all oxide TFT/Fe-FET.

1. $SiO_2$/Si substrate cleaning
2. ALD 30 nm $HfO_2$
3. ALD 20 nm $Al_2O_3$ as spacer
4. ALD 10 nm $In_2O_3$ as gate electrode
5. ALD 10 nm $Al_2O_3$ as spacer (★)
6. Trenching by dry etching (★)
7. ALD gate oxides
8. ALD $In_2O_3$ at as channel
   - ❖ PDA in $N_2$, 400 ℃ (for Fe-FETs)
9. Channel isolation by dry etching
10. Gate region exposure by dry/wet etching
11. PDA in $O_2$

Fig. 3. Fabrication process flow of all-oxide planar or vertical TFTs and Fe-FETs based on ALD $In_2O_3$. The steps in star are special for vertical structure.

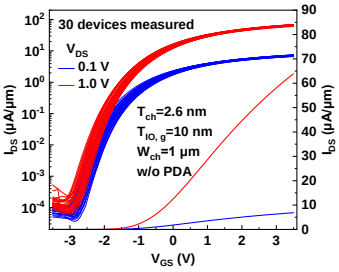


Fig. 4 $I_D$-$V_{GS}$ characteristics of 30 all-oxide TFTs randomly from four 0.5-by-0.5-μm dies.

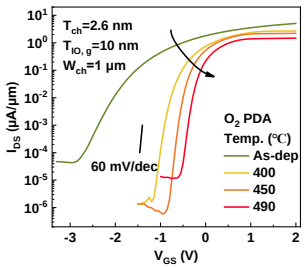


Fig. 5 Evolution of $I_D$-$V_{GS}$ characteristics of a full-oxide planar TFT with PDA at various temperatures.

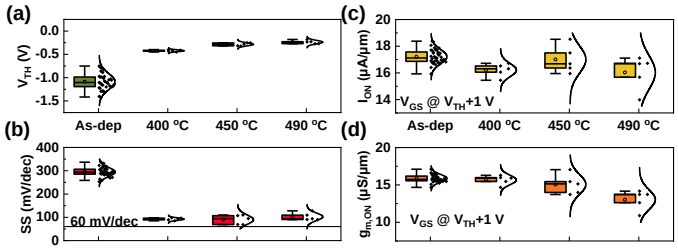


Fig. 6. Statistical plots of (a) $V_{TH}$, (b) SS, (c) $I_{ON}$ and (d) $g_{m,ON}$ for as-deposited all-oxide TFTs and devices with PDA at temperature from 400 to 490 °C.

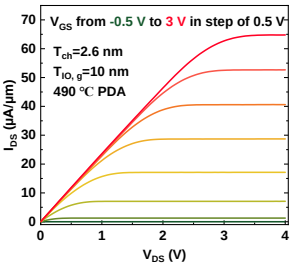


Fig. 7. $I_D$-$V_{DS}$ characteristics of an all-oxide TFT with $L_{ch}$ of 2 μm, $T_{ch}$ of 2.6 nm, and PDA at 490 °C.

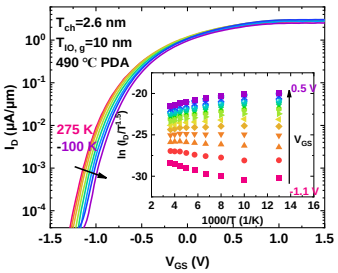


Fig. 8. Temperature-dependent $I_D$-$V_{DS}$ characteristics of a full-oxide TFT from 275 to 100 K. Inset: Arrhenius plot at different gate biases.

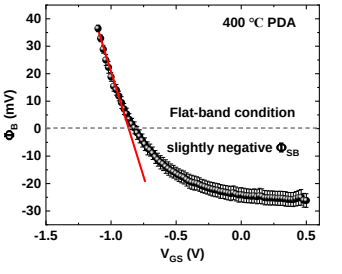


Fig. 9. Extracted $\Phi_B$ as a function of $V_{GS}$. $\Phi_{SB}$ is extracted at flat-band condition.

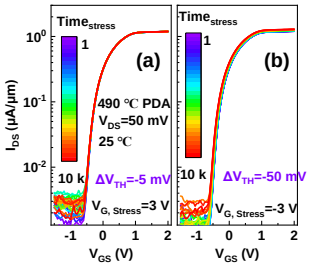


Fig. 10. Evolution of transfer curves of an all-oxide $In_2O_3$ TFT with PDA at 490 °C under (a) PBS of 3 V and (b) NBS of -3 V for $10^4$ s.

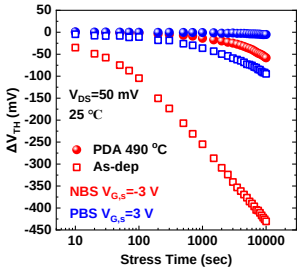


Fig. 11. Time evolution of $\Delta V_{TH}$ of a full-oxide TFT with and without PDA under PBS and NBS for $10^4$ s.

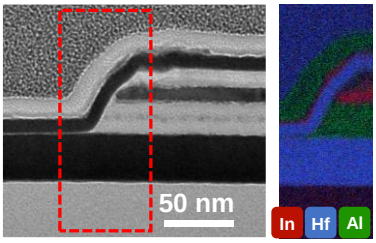


Fig. 12. HRTEM cross-section image and EDS mapping of an ALD vertical all-oxide FET with $T_{IO,g}$ of 10 nm.

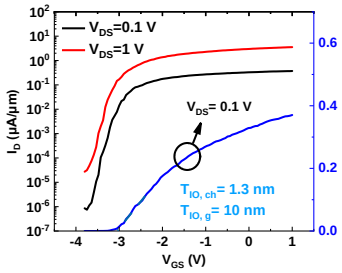


Fig. 13. Transfer curves of an ALD vertical all-oxide FET with $L_{ch}$ of 16 μm, $T_{IO,ch}$ of 1.3 nm and $T_{IO,g}$ of 10 nm.

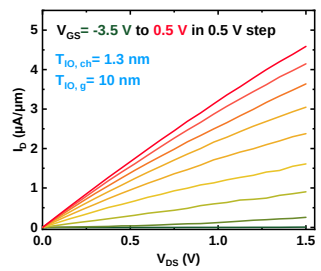


Fig. 14. Output curves of same device as Fig. 13. The low drain is due to a long channel of 16μm.

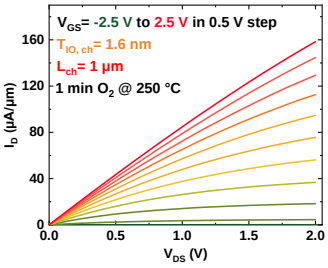


Fig. 15. Output curves of an ALD vertical all oxide FET with $L_{ch}$ of 1 μm, $T_{IO,ch}$ of 1.3 nm and $T_{IO,g}$ of 10 nm.

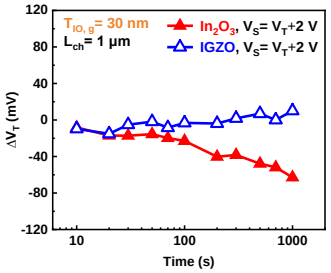


Fig. 16. Time evolution of $\Delta V_{TH}$ of vertical full-oxide TFTs based on $In_2O_3$ and IGZO under PBS for $10^3$ s.

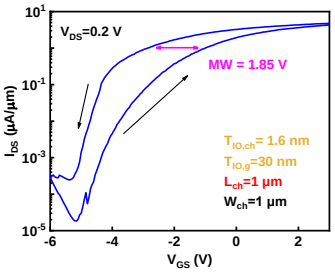


Fig. 17. $I_D$-$V_{GS}$ characteristics of an ALD vertical $In_2O_3$ Fe-FET with $T_{IO,ch}$ of 1.6 nm, $T_{IO,g}$ of 30 nm and $L_{ch}$ of 1 μm.

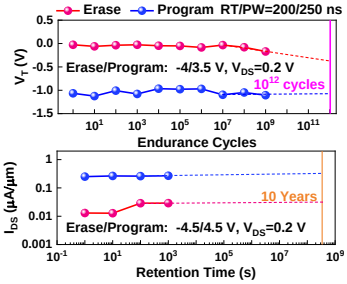


Fig. 18. Major states endurance and retention performance of an ALD vertical $In_2O_3$ Fe-FET at room temperature.